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Design of 2.5-Micrometer Josephson Current Injection Logic (CIL)

This paper describes Josephson Current Injection Logic (CIL) circuits. The design of the basic logic circuits, the two- and four-input OR and AND gates, and a timed inverter circuit, is presented in full detail and the logic delay and its sensitivity to design and fabrication parameters are investigated using detailed models of devices based on a 2.5-μm technology. The nominal logic delay of the circuits is estimated at 36 ps per gate for an average fan-in of 4.5 and fan-out of 3. The corresponding average power dissipation is 3.4 microwatts per gate. Finally, experimental delay measurements are presented for two-input and four-input OR and AND gates. The delay experiments are in excellent agreement with computer simulations.

Introduction

This paper reports detailed designs of the Current Injection Logic (CIL) family [1, 2] consisting of two-input OR, two-input AND, four-input OR, four-input AND, and two-input EXCLUSIVE-OR (XOR) gates, as well as a timed inverter circuit. (Note: Some material similar to that reported previously in [1] and [2] is included in this paper for completeness.) A review of the earlier work on Josephson logic circuits including latches and inverters and an explanation of logic devices can be found in a paper by Matisoo in this issue or in the references [1-7]. The CIL circuits combine both the magnetically coupled interferometers (also known as SQUIDs—superconducting quantum interference devices) [8] and current injection gates [1] to obtain smaller switching delays, wider operating margins, and greater fan-in and fan-out capabilities. The following sections describe the devices used in the logic circuits, the basic logic circuits, the detailed design of the 2.5-μm CIL, the performance of the 2.5-μm CIL based on computer simulations, and experimental verification of the 2.5-μm CIL performance.

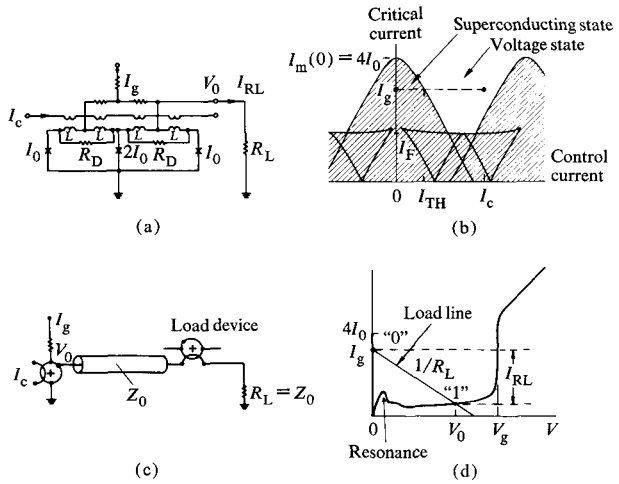

Figure 1 (a) Three-junction I_0:$2I_0$:I_0, split-feed interferometer. (b) Threshold curve of the three-junction interferometer. (c) Schematic representation of a three-junction interferometer as a switching device with matched, superconducting transmission line and a serially connected load device. (d) *I-V* curve of the interferometer and the load line indicating the switching between the superconducting state corresponding to the "0" logic level and the voltage state V_0 corresponding to the logic level "1."

Devices

Two types of devices are used in the CIL circuits: a three-junction magnetically coupled interferometer [8] shown in Fig. 1, and a two-junction asymmetric injection gate [1] shown in Fig. 2. In the "0" state, the three-junction interferometer is biased in the superconducting state by a gate current $I_g < I_m(0)$, where $I_m(0)$ is the critical current of the interferometer for zero control current, equal to $4I_0$, where I_0 is the critical current of the Josephson junction. When a magnetically coupled control current I_c is applied

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to the interferometer, it switches to a voltage V_0 representing a logic "1" state and directs its gate current into the load resistor R_L [Figs. 1(a) and (c)]. The modulation of the interferometer critical current by the control current is indicated by the threshold curve of Fig. 1(b). The minimum control current needed to switch the interferometer is called the threshold current I_{TH}. The output current I_{RL} is determined by the *I-V* curve of the interferometer and the load resistor R_L [Fig. 1(d)]. For normal operation of the interferometer, the load resistor R_L and the interferometer critical current $4I_0$ are selected to maximize the output current I_{RL} by obeying

$$4I_0R_L < V_g. \tag{1}$$

The gap voltage V_g is $\approx$3 mV for the lead-alloy technology used to fabricate the CIL circuits. The internal resonances of the interferometer are damped by resistors R_D such that the load line does not intersect the resonance peak [9].

The other device used in the CIL logic family is the injection gate shown in Fig. 2. There are two input currents, I_A and I_B, both of which are directly injected into the injection gate. The operating margin of the injection gate is optimized by selecting its critical currents and inductances such that the following two equations are obeyed:

$$L_1I_{01} = L_2I_{02}; \tag{2}$$

$$(L_1 + L_2)I_{02} = \Phi_0 = \frac{h}{2e}\text{, a flux quantum.} \tag{3}$$

Under these conditions the input current I_A required to switch the injection gate to a voltage state is a nonlinear function of the input current I_B as shown by the threshold curve of Fig. 2(b). In particular, the current needed to switch the interferometer when both inputs are applied simultaneously is about one-third of the current required when only either one of the inputs is applied. Thus the injection gate functions as a two-input AND gate. A resistor R_D is used to damp the injection gate.

The three-junction interferometers and the injection gates are used for specific functions in the CIL circuits, as will be described in the following section. The three-junction interferometer provides isolation through magnetically coupled control lines and a two-input OR function by incorporating two control lines, either of which can switch the interferometer to the voltage state when activated. On the other hand, the injection gate is used to provide AND functions and high gain by directing both injected currents to the output load. The high gain in turn is used to obtain small logic delays and wide margins and to provide a parallel fan-out capability.

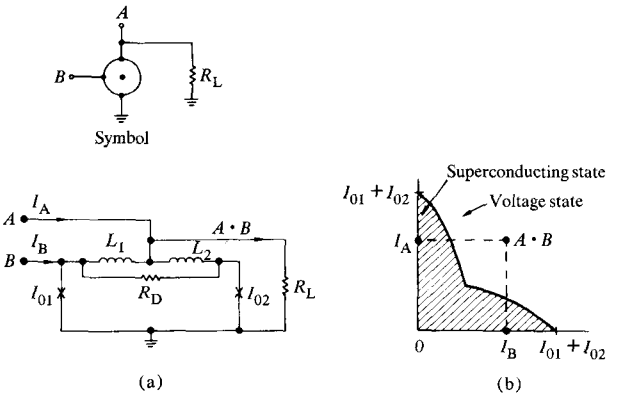

Figure 2 (a) Two-junction injection gate and its symbol. (b) Nonlinear threshold curve of the injection gate performs the $A \cdot B$ function. The injection gate switches to the voltage state only when both the inputs I_A and I_B are *on*.

CIL circuits

The four basic CIL circuits are the two- and four-input OR and AND gates shown in Fig. 3. The two-input OR gate shown in Fig. 3(a) is essentially the same as the one reported earlier by Klein and Herrell [4] consisting of a three-junction interferometer Q_1 with two control lines *A* and *B*, either of which can switch the interferometer to the nonzero voltage state when activated. The control lines of the load devices are connected in series with the output transmission line which is terminated in a matching resistor $R_L = Z_0$. The two-input AND gate [Fig. 3(b)] consists of two three-junction interferometers, Q_2 and Q_3, and an injection gate G_1. The injection gate switches only when both interferometers are switched to the voltage state. Thus the overall function of the two-input AND gate of Fig. 3(b) is $(A_1 + A_2) \cdot (B_1 + B_2)$. By proper choice of input signals one can obtain the XOR function, $(A + B) \cdot (\bar{A} + \bar{B})$. The four-input OR gate [Fig. 3(c)] is comprised of two three-junction interferometers Q_4 and Q_5 and small resistors R_C connecting their end junctions. When interferometer Q_4 is switched by application of control *A*, for example, it switches its gate current into the interferometer Q_5 via the resistors $R_C(R_C << R_{L1} = R_{L2})$, switching interferometer Q_5 into the voltage state. The gate currents of interferometers Q_4 and Q_5 are then both switched to the parallel loads R_{L1} and R_{L2}. The two outputs add parallel fan-out capability to the serial fan-out capability of CIL circuits. The four-input AND circuit [Fig. 3(d)] consists of two two-input AND gates, the outputs of which are injected into a large injection gate G_4. To allow for larger input currents the injection gate G_4 has junctions with larger critical currents than the injection gates used in two-input AND gates. All four three-junction interferometers must switch in order to obtain an output from the four-input AND gate. The output current is suffi-

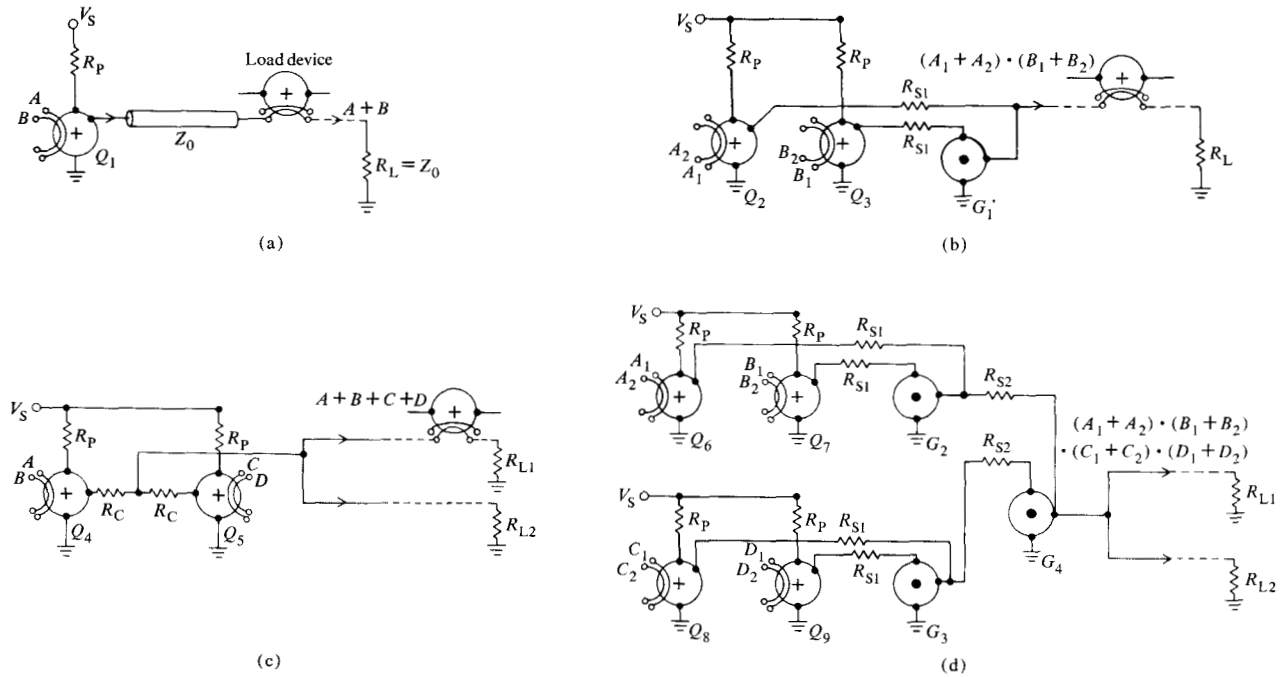

Figure 3 CIL circuits: (a) Two-input OR gate, (b) two-input AND gate which also performs the EXCLUSIVE-OR function $(A + B) \cdot (\bar{A} + \bar{B})$, (c) four-input OR gate, and (d) four-input AND gate. [Circles with + (OR) signs represent the three-junction interferometers and the circles with • (AND) signs represent the injection gates.]

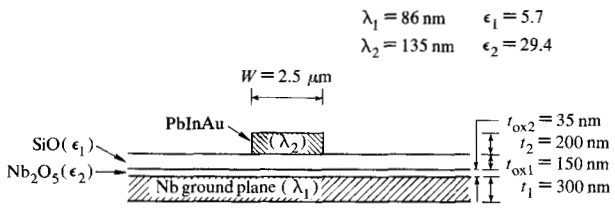

Figure 4 Cross-section of a 2.5-μm, 12-Ω transmission line over a superconducting ground plane.

ciently large to allow two loads, R_{L3} and R_{L4}, in parallel. The four-input AND gate also has a two-input OR gate at each input for a total fan-in of eight.

Design of 2.5-μm CIL circuits

• *Transmission lines*

The logic signals are carried over transmission lines formed by 2.5-μm superconducting lines over a superconducting ground plane, separated by two levels of insulators, an example of which is shown in Fig. 4. The characteristic impedance Z_0 and the propagation delay per micrometer t_p' are approximated by the following formulae [10]:

$$Z_0 = \sqrt{\frac{L}{C}} \quad \text{and} \quad t_p' = \sqrt{LC} \tag{4}$$

where L is the inductance per unit length of the superconducting transmission line given by

$$L = \frac{\mu_0}{kW}\left(t_{ox1} + t_{ox2} + \lambda_1 \coth\frac{t_1}{\lambda_1} + \lambda_2 \coth\frac{t_2}{\lambda_2}\right),$$

C is the capacitance per unit length of the transmission lines formed by two insulators in series, given by

$$C = \frac{k\epsilon_0 W}{\left(\frac{t_{ox1}}{\epsilon_1} + \frac{t_{ox2}}{\epsilon_2}\right)},$$

and

W = width of the superconducting transmission line,

λ_1 and λ_2 = superconducting penetration depths of the ground plane and the transmission line,

t_1 and t_2 = thicknesses of the ground plane and the transmission line,

t_{ox1} and t_{ox2} = thicknesses of the insulation levels,
ϵ_1 and ϵ_2 = dielectric constants of the insulation levels,
μ_0 = permeability of free space, and
k = fringing factor.

For the 2.5-μm lines illustrated in Fig. 4 the fringing factor is approximately 1.3 [11]. The transmission line parameters for this line are

$$Z_0 = 12\ \Omega \text{ and } t_p' = 0.012\ \text{ps}/\mu\text{m}. \quad (5)$$

• *Three-junction interferometer design*

The critical current I_0 for the three-junction interferometer was chosen to be 50 μA to satisfy Eq. (1) with a load resistor $R_L = 12\ \Omega$. The next step was to determine the loop inductance $2L$ of the interferometer, which involves a trade-off between the gain of the interferometer and its gate current margins. The control current I_c needed to switch the interferometer decreases as the loop inductance L is increased, but the floor of the threshold curve I_F [see Fig. 1(b)], which determines the lower limit of the allowed gate current variation, increases as L is increased. The trade-off is shown graphically in Fig. 5. A loop inductance of 12 pH was chosen to minimize I_{TH} and to allow adequate gate current margins.

The essential details of the layout and the vertical structure of the three-junction interferometer are shown in Fig. 6. The minimum linewidths and level-to-level alignments used in the layout are 2.5 μm. The loop inductance of the interferometer is formed mainly by the base electrode which passes over holes in the ground plane to increase its inductance per unit length and hence to reduce the size of the three-junction interferometer and its parasitic capacitance to the ground plane [12]. There are two control lines over the interferometer.

The ground plane holes used to increase the inductance provide sites where ambient magnetic flux can be trapped when the ground plane is cooled below its critical temperature. This in turn would distort the threshold curve and cause inadvertent switching of the interferometers. For the delay experiments reported in subsequent sections this problem was eliminated by placing a niobium plate at the back of the test chip as an additional ground plane and by orienting the test chip in such a way as to reduce the magnetic field threading it before it is cooled below the critical temperature.

A detailed model of the three-junction interferometer is shown in Fig. 7. The Stewart-McCumber model shown in Fig. 7(a) is used for the Josephson junctions [13, 14]. The subgap resistance R_j of the Josephson tunnel junctions is characterized by a process- and materials-dependent voltage $V_m = I_0 R_j$. For the lead-alloy process [15] used in the 2.5-μm CIL design, $V_m \approx 27$ mV. The inductances and parasitic capacitances of the three-junction interferometer are estimated from the layout of Fig. 6. The portion of the loop inductance coupled to the control line, L_m, is 86 percent of the total loop inductance $L_T = L_m + L_k + L_s$. That portion of the kinetic inductance of the superconductors which does not magnetically couple to the control line is L_k, and L_s is the inductance of the counter electrode which does not couple because it is at right angles to the control line. The total inductance of the control

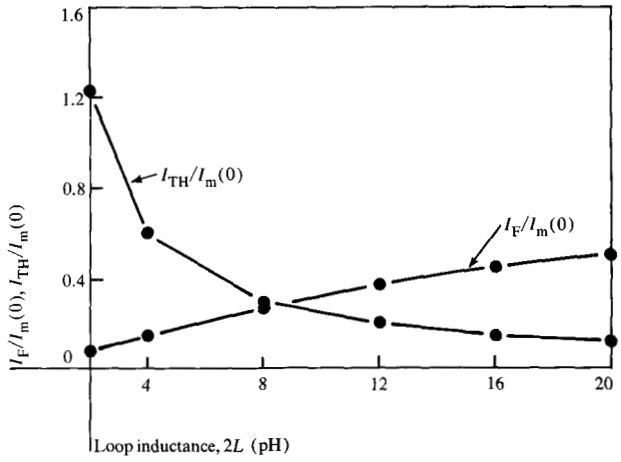

Figure 5 Gain-margin trade-off for the three-junction interferometer. The normalized control current $I_{TH}/I_m(0)$ required to switch the interferometer at the gate current $I_g = [I_m(0) + I_F]/2$ and the normalized floor current $I_F/I_m(0)$ are plotted as a function of the interferometer loop inductance $2L$.

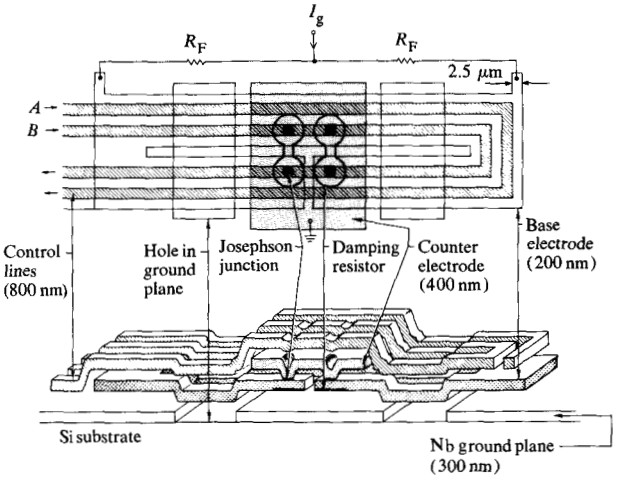

Figure 6 Salient features of the layout and vertical structure of the three-junction interferometer.

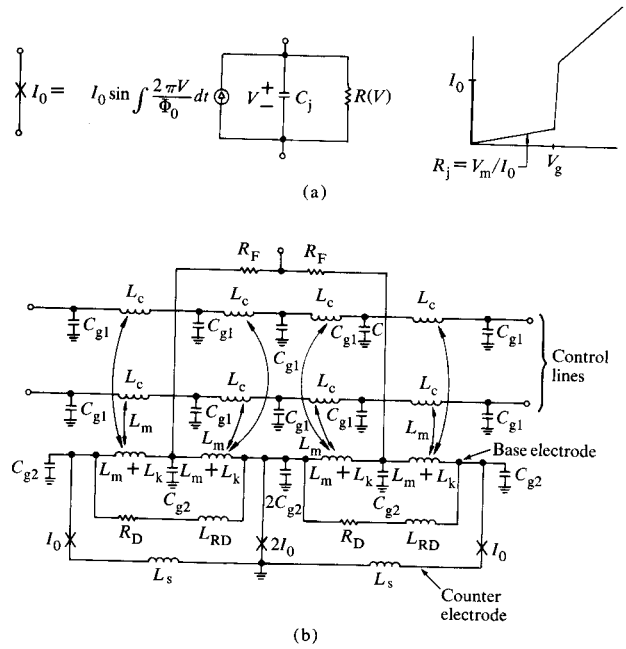

Figure 7 (a) Stewart-McCumber model for a point Josephson junction. (b) The model for a three-junction interferometer with two control lines. (I_0 = 50 μA, C_j/I_0 = 3.4 pF/mA, L_k = 0.6 pH, L_m = 5.4 pH, L_c = 13 pH, L_s = 0.6 pH, C_{g1} = 0.1 pF, C_{g2} = 0.14 pF, R_F = 20 Ω, R_D = 3.2 Ω, L_{RD} = 0.4 pH.)

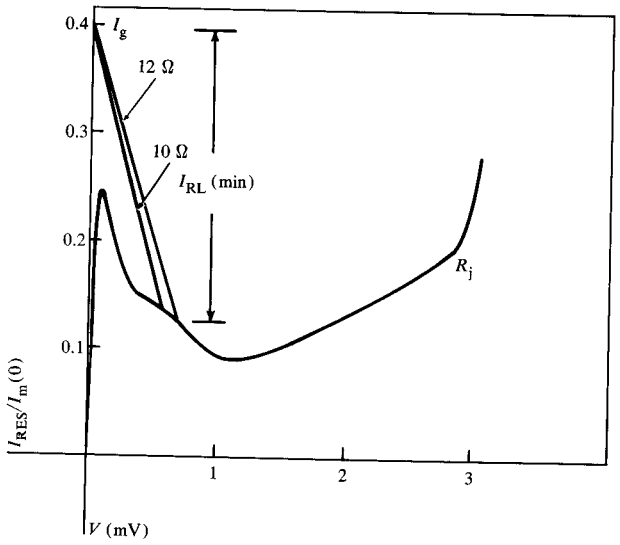

Figure 8 Normalized resonance amplitude of the three-junction interferometer and two load lines (R_L = 12 Ω and 10 Ω) at the minimum allowable gate current I_g(min) = I_F = 0.4I_m(0).

line is 4L_c. The optimum value of R_D was determined to be 3.2 Ω with associated inductance L_{RD} of 0.4 pH. The resultant resonance steps for the damped three-junction interferometer and the load line for the worst-case current I_g (min) = 0.4 I_m(0) are shown in Fig. 8. The output current into a 12-Ω load for the above worst case is 54 μA, enough to exceed the nominal threshold current I_{TH} (= 44 μA). The three-junction interferometer is nominally biased at a gate current I_g = [I_m(0) + I_F]/2 = 140 μA. The nominal output current into a 12-Ω load is 110 μA.

• *Design of small injection gates*

The sum of the critical currents of the small injection gate (Fig. 2) is determined by the amplitude of the injection currents I_A and I_B. For optimum margins the injection current is made equal to 0.6(I_{01} + I_{02}), about halfway between the maximum allowable value of I_{01} + I_{02} and the minimum allowable value of 0.32(I_{01} + I_{02}). The injection current for the two-input AND gate of Fig. 3(b) is 120 μA for a load resistor R_{S1} = 10 Ω. [The 10-Ω value of R_{S1} is selected to clear the resonance peak of the three-junction interferometer (see Fig. 8) as well as to maximize the output current of the two-input AND gate.] Thus I_{01} + I_{02} = 200 μA.

The ratio I_{02}/I_{01} for the injection gate is determined by two considerations. The first consideration is to maximize the operating region of the injection gate by minimizing the threshold current when both inputs are *on*. The threshold current to switch the injection gate when both the injection currents are *on* is plotted as a function of the I_{02}/I_{01} ratio in Fig. 9. It is seen that the optimum value of the ratio lies between about 1.5 and 4. The second consideration is that the total inductance $L_1 + L_2 = \Phi_0/I_{02}$ [from Eq. (3)] and consequently the size of the injection gate can be minimized by making I_{02} large. However, for a given current density the minimum value of I_{01} is limited to the critical current I_0 of the 2.5-μm-diameter Josephson junctions of the three-junction interferometer. Thus:

$$I_{01} = 50\ \mu\text{A and } I_{02} = 150\ \mu\text{A}, \tag{6}$$

and from Eqs. (2) and (3)

$$L_1 = 10.35\ \text{pH and } L_2 = 3.45\ \text{pH}.$$

The layout and the vertical structure of the small injection gate are shown in Fig. 10(a). The loop inductance of the injection gate is formed by the base electrode as before. However, instead of a hole in the ground plane, steps of oxides separating the base electrode from the ground plane are used to increase the inductance of the base electrode. Because there are no control lines over the injection gate, it is considerably smaller than the three-junction interferometer of Fig. 6. The damping resistor R_{D2} is designed such that the injection gate does

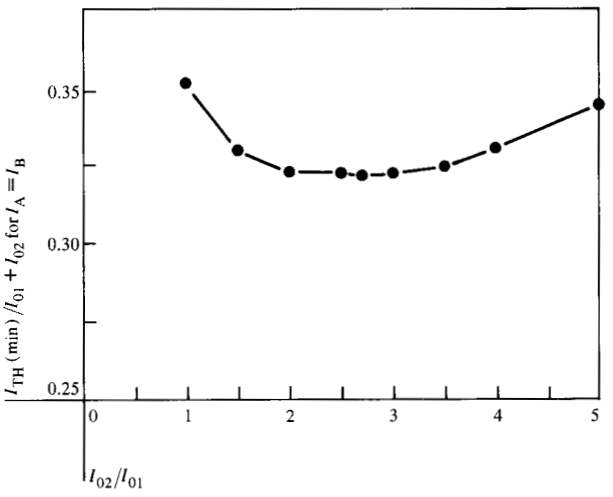

Figure 9 Minimum injection current ($I_A = I_B$) required to switch the injection gate as a function of $N = I_{02}/I_{01}$.

not erroneously switch into the voltage state when a quantum of flux Φ_0 is entered into the loop by injection of the asymmetric input I_B [1]. The damping resistor was optimized to 3.5 Ω using computer simulations. The equivalent circuit of the small injection gate is shown in Fig. 10(b).

Design of the large injection gate

The large injection gate is used in the four-input AND gate of Fig. 3(d). The injection current fed into the large injection gate G_4 is the output of the two-input AND gate into a load $R_{S2} = 5\ \Omega$, equal to 180 μA. The 5-Ω value of R_{S2} is selected to clear the resonance of the small injection gates and to maximize the output current of the four-input AND gate. Following the same design process as for the small injection gate above, we obtain for the large injection gate

$$I_{01} = 50\ \mu A,\ I_{02} = 250\ \mu A,\ L_1 = 6.9\ pH,$$
$$L_2 = 1.38\ pH,\ \text{and}\ R_{D3} = 12.5\ \Omega. \quad (7)$$

The model for the large injection gate is shown in Fig. 11. Its layout and vertical structure are similar to those of the small injection gate shown in Fig. 10(a).

Performance of 2.5-μm CIL circuits

Computer simulations based on the device models described in the preceding section were used to estimate the logic delay and its sensitivity to some design variables. The total logic delay t_D was separated into three components:

$$t_D = t_g + t_p + t_x, \quad (8)$$

where t_g is the time required to switch the interferometer from the superconducting state into the nonzero voltage

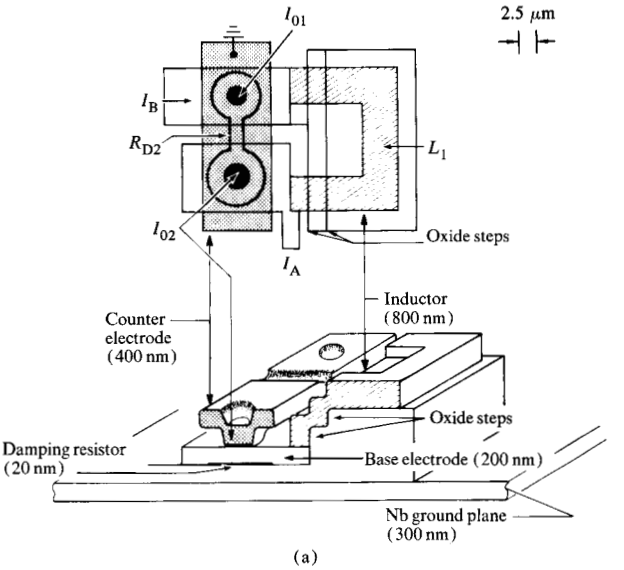

Figure 10 (a) Layout and vertical structure of the small injection gate. (b) Model of the small injection gate. ($I_0 = 50\ \mu A$, $L_1 = 3.45$ pH, $L_s = 0.6$ pH, $R_{D2} = 3.5\ \Omega$, $L_{R_{D2}} = 0.4$ pH.)

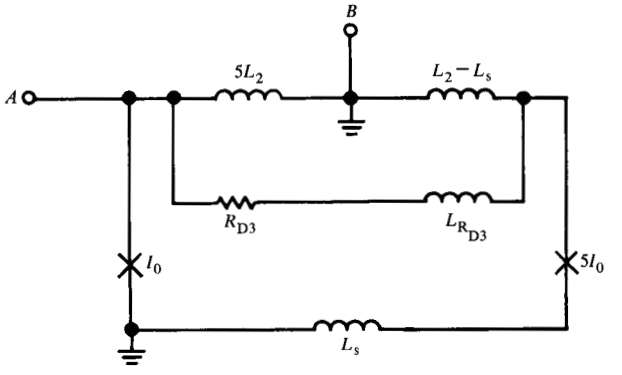

Figure 11 Model for the large injection gate. ($I_0 = 50\ \mu A$, $L_2 = 1.38$ pH, $L_s = 0.5$ pH, $R_{D3} = 2.5\ \Omega$, $L_{R_{D3}} = 0.3$ pH.)

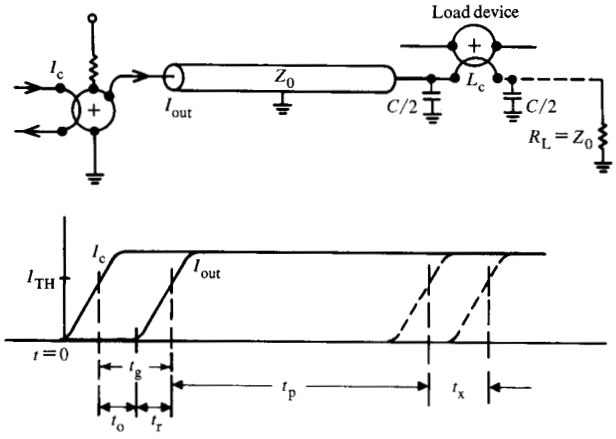

Figure 12 Delay components of Josephson logic: t_o = turn-on delay, t_r = rise time, t_p = propagation delay, and t_x = crossing delay.

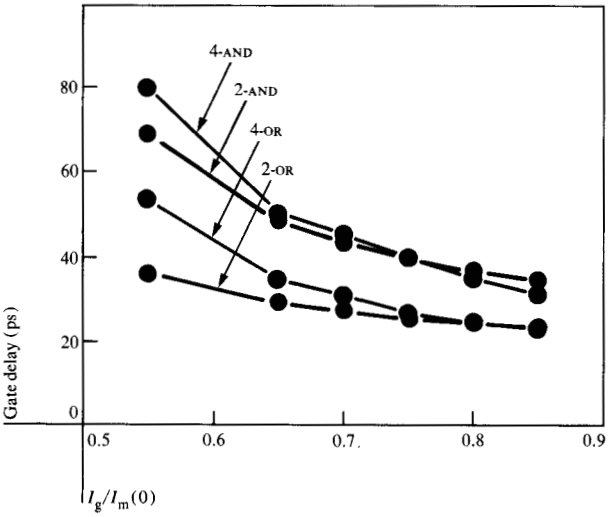

Figure 13 Logic delay estimates of CIL circuits as a function of the normalized gate current.

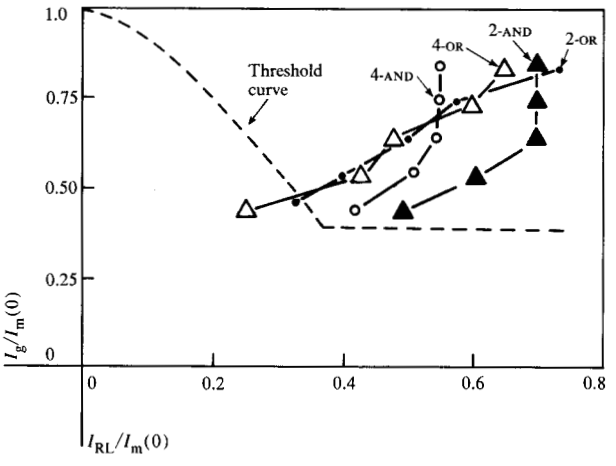

Figure 14 Normalized output currents $I_{RL}/I_m(0)$ of the CIL circuits are shown plotted against normalized gate current $I_g/I_m(0)$.

state. It consists of two components, the turn-on delay t_o [16] and the rise time t_r as shown in Fig. 12. The propagation delay t_p is the time of flight of the signal to the load device. The crossing delay t_x is the time required for the signal to cross a load device, and is given [8] by

$$t_x = \frac{L_x}{Z_0}, \tag{9}$$

where L_x is the crossing inductance of the control line, equal to $4L_c$ as shown in Fig. 7. For signal rise times greater than $3L_x/Z_0$, the crossing inductance can be adequately matched to the transmission line using matching capacitors, shown in Fig. 12, and given by

$$C = \frac{L_x}{Z_0^2}. \tag{10}$$

The propagation delay t_p and the crossing delay t_x together constitute the fan-out delay and are, as such, dependent on the system architecture, circuit density, chip partitioning, etc. Based on prior experience, however, it is possible to argue that on the average a logic gate will have a fan-out of about three. Further, the average transmission line length for an on-chip serial fan-out of three is estimated to be about 500 μm [17] for a 2.5-μm CIL logic chip measuring 6.35 mm on a side and containing a total of one thousand logic gates. For logic gates with two parallel outputs the propagation delay and the crossing delay are about half. The rise time will also be reduced to one-half for the parallel fan-out gate because of the smaller load resistance of $Z_0/2$. Thus, for L_x = 52 pH, Z_0 = 12 Ω and t_p' = 0.012 ps/μm, the average fan-out delay for a fan-out of three is estimated to be

$$t_x + t_p = 14.7 \text{ ps for two-input OR and two-input AND gates} \tag{11}$$

or

$$t_x + t_p = 7.4 \text{ ps for four-input OR and four-input AND gates.}$$

The results of computer simulations to estimate the total logic delay t_D of nominal CIL gates are shown in Fig. 13 as a function of the normalized gate current $I_g/I_m(0)$. The logic delay is a strong function of the gate current for two reasons. As the gate current increases, not only does the output current I_{RL} increase but the threshold current required to switch the three-junction interferometer decreases. This is illustrated graphically in Fig. 14, where the output currents I_{RL} of the CIL gates are plotted against the gate current. The threshold curve of the three-junction interferometer is superimposed using dotted lines to show the threshold current I_{TH} required to switch a load device at the same gate current. In the case of the four-input OR and four-input AND gates the output current

plotted is the current in each of the two parallel outputs. The output currents of the two-input AND and the four-input AND gates are clamped to 140 μA and 110 μA respectively because the three-junction input interferometers switch to the gap voltage for gate currents exceeding 0.6 $I_m(0)$.

The nominal gate current level in the three-junction interferometers is set at 0.7 $I_m(0)$ to maximize the margins on the gate current and on the critical currents of the three-junction interferometer. The total logic delay of the CIL circuits and their delay components at the nominal gate current are summarized in Table 1. The power dissipation of each logic gate is also listed in Table 1, assuming a 12-mV ac power supply with an 80% duty cycle [18]. The power dissipation in the on-chip voltage regulators is not included in these calculations. Thus the nominal logic delay of the CIL circuits averaged over the OR and the AND gates is about 36 ps/gate and the average power dissipation is 3.4 μW. The sensitivity of the logic delay to junction capacitance C_j, critical current I_0, subgap tunneling characteristic V_m, damping resistor R_D, and load impedance Z_0 is reported below.

• *Logic delay sensitivity*

To study the effect of the junction capacitance, the switching delay t_g was estimated for the nominal, twice the nominal, and three times the nominal junction capacitance. As shown in Fig. 15, the switching delay is very sensitive to the junction capacitance. The fan-out delay is independent of the junction capacitance. The parasitic capacitances of the devices were left unchanged in these delay simulations.

To study the effect of the critical current I_0 on the logic delay, the two-input OR gate was redesigned with I_0 = 60 μA. The loop inductance was decreased to 10 pH to maintain the same LI_0 product as before, and the gate current was increased to maintain a nominal bias of 0.7 $I_m(0)$. The results of the computer simulations, shown in Fig. 16, indicate that the logic delay of the two-input OR gate with higher I_0 does not differ from the nominal design. The crossing delay t_x for the higher critical current is slightly smaller because of lower crossing inductance L_x = 48 pH associated with the lower loop inductance of the three-junction interferometer. With the higher critical current, the power dissipation and the power supply current handling requirements will increase proportional to I_0.

The subgap resistance, defined as $R_j = V_m/I_0$ of the Josephson junction, determines the output current and hence the gain and the speed of the logic circuits, where V_m is a materials-dependent parameter. The output cur-

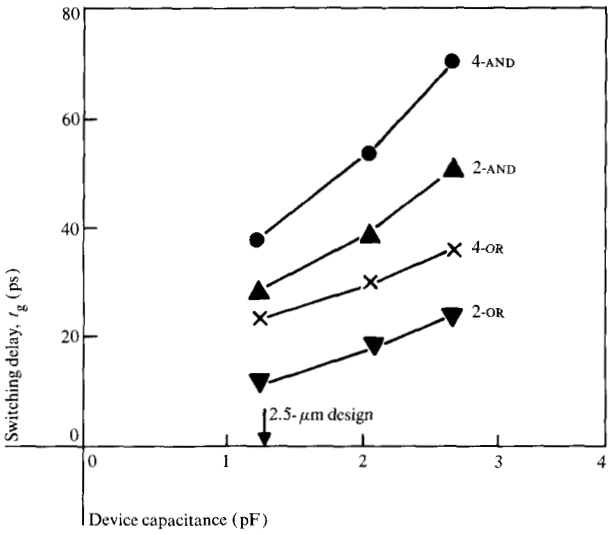

Figure 15 Nominal switching delay t_g as a function of device capacitance.

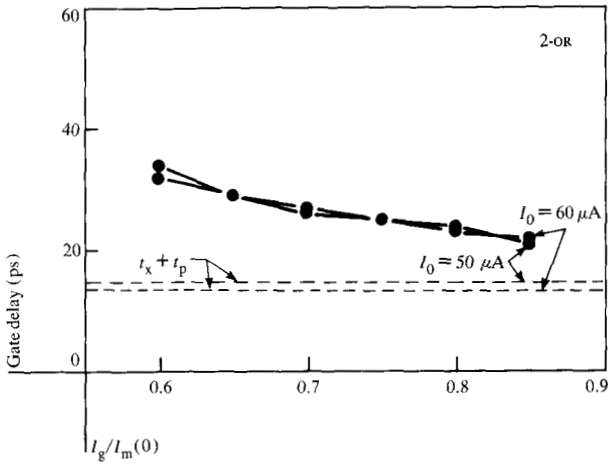

Figure 16 Comparison between the logic delay of a CIL two-input OR gate for two critical current values I_0 = 50 μA and I_0 = 60 μA.

Table 1 Simulated logic delay and power dissipation of 2.5-μm CIL circuits.

Gate	*Logic delay* (ps) *for* $I_g = 0.7\ I_m(0)$				*Power dissipation* (μW)
	t_D	t_g	t_p	t_x	
2-OR	27	12.3	6	8.7	1.5
4-OR	27	19.6	3	4.4	3.0
2-AND	43	28.3	6	8.7	3.0
4-AND	45	37.6	3	4.4	6.0
Average	35.5	24.5	4.5	6.5	3.4

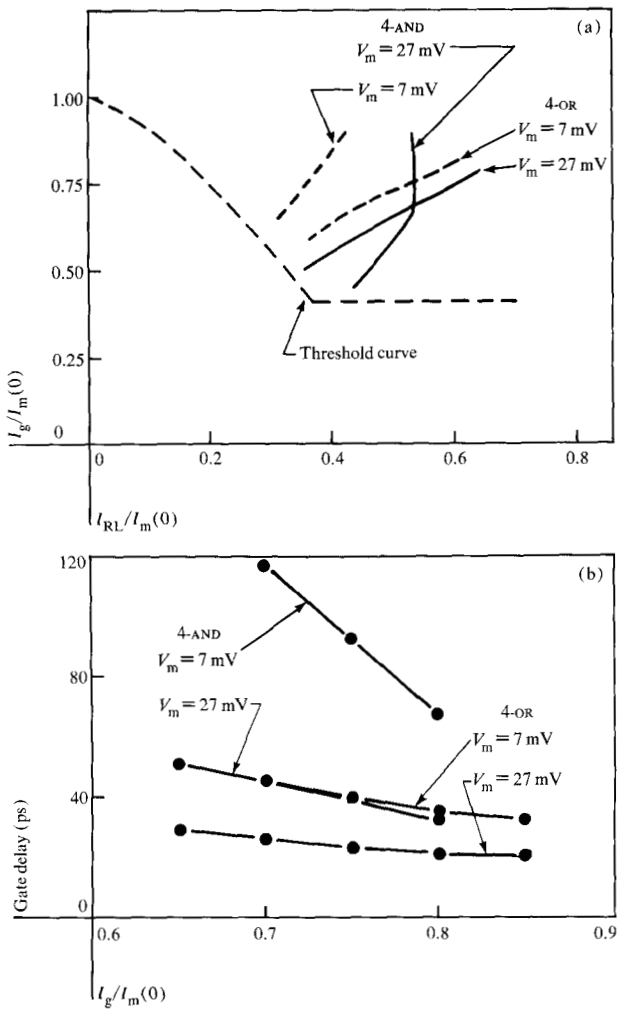

Figure 17 Effect of the subgap tunneling resistance R_j on the performance of the CIL circuits: (a) output currents of CIL four-input OR and four-input AND gates for $V_m = 27$ mV and $V_m = 7$ mV; and (b) the logic delay of the same logic gates for $V_m = 27$ mV and $V_m = 7$ mV.

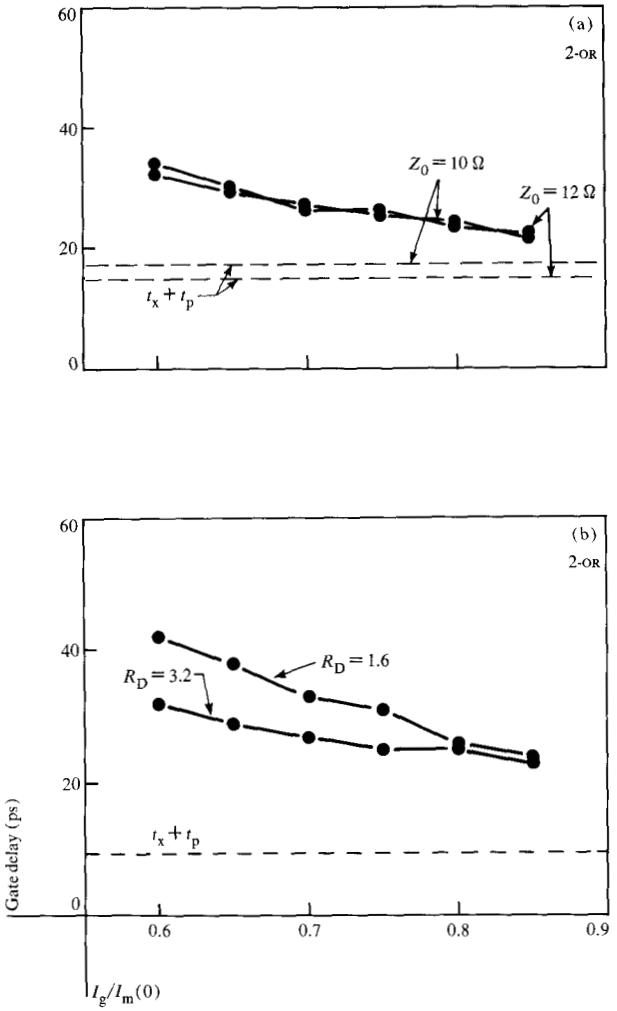

Figure 18 (a) Logic delay estimates for two values of characteristic impedance, $Z_0 = 12\ \Omega$ and $10\ \Omega$. (b) Logic delay for two values of the three-junction interferometer damping resistors $R_D = 3.2\ \Omega$ and $1.6\ \Omega$.

rents and the logic delay were estimated for the four-input OR and four-input AND gates for $V_m = 27$ mV corresponding to the standard lead-alloy process, and for $V_m = 7$ mV corresponding to a poor quality junction. The corresponding subgap tunneling resistances R_j of the three-junction interferometer are 135 Ω and 35 Ω, respectively. The normalized output currents for the two cases are compared in Fig. 17(a). The loss of output current amplitude is more evident in the four-input AND gate, which has more Josephson junctions in parallel with the load resistors than the four-input OR gate. The threshold curve is superimposed on Fig. 17(a), using dotted lines to indicate the lower gain, I_{RL}/I_{TH} for the lower V_m case. The larger logic delay caused by the lower output current is illustrated in Fig. 17(b). There is no further significant improvement in the logic delay if the V_m is increased beyond 27 mV.

The effects of the transmission line impedance Z_0 and the three-junction interferometer damping resistor R_D on the logic delay of the two-input OR gate are indicated in Figs. 18(a) and 18(b), respectively. The reduction in the rise time t_r because of lower transmission line impedance $Z_0 = 10\ \Omega$ is compensated by the increase in the crossing delay t_x. Overall, as seen from Fig. 18(a), the logic delay has a very weak dependence on Z_0. If the damping resistor is made too small, the logic delay increases significantly through large turn-on delay t_0 [Fig. 18(b)]. How-

ever, it is found that the improvement in the logic delay is insignificant if R_D is increased beyond 3.2 Ω.

Thus we can conclude from the above discussion that the logic delay is strongly dependent upon two factors: the capacitance of the Josephson junctions, C_j, and the gate current level, $I_g/I_m(0)$. The latter in turn is determined by the processing variations in the maximum critical current of the interferometer, $\Delta I_m(0)$ such that $I_g(\max) < [I_m(0) - \Delta I_m(0)]$. The subgap resistance of the Josephson junction is not critical for $V_m \approx 27$ mV but it does contribute significant delay for small values of V_m. Similarly, small variations in the damping resistor R_D do not change the logic delay significantly for $R_D \approx 3.2$ Ω, but at low values of R_D (≈1.6 Ω) there is a significant increase in the logic delay.

• *Punchthrough speed of CIL circuits*

The CIL circuits described in this paper are latching, which implies that, once switched into the voltage state, they do not reset to the superconducting state when the control current is removed. The resetting is achieved through an alternating power supply current [18] shown in Fig. 19. The logic circuits in the *on* state are reset to a superconducting state when the power supply crosses zero. There is a lower limit, however, on the power supply transition time τ_t below which there is a nonzero probability that the circuit will not reset to the superconducting state but "punch through" into the voltage state [19]. The punchthrough speed of the CIL circuits was estimated using computer simulations. To reduce the computation costs the logic circuit outputs were directly terminated into a 12-Ω load without any fan-out load. The following lower limits are estimated on τ_t, above which proper resetting will occur:

$\tau_t \geq 130$ ps for OR gates, and

$\tau_t \geq 250$ ps for AND gates. (12)

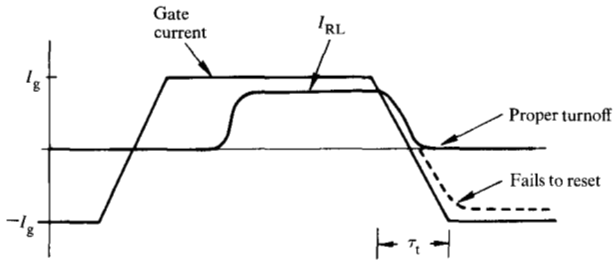

Figure 19 The ac power supply, which resets the latching logic circuits from the nonzero voltage state to the superconducting state at the end of every cycle. The transition time of the power supply τ_t must not exceed the punchthrough speed of the logic circuits.

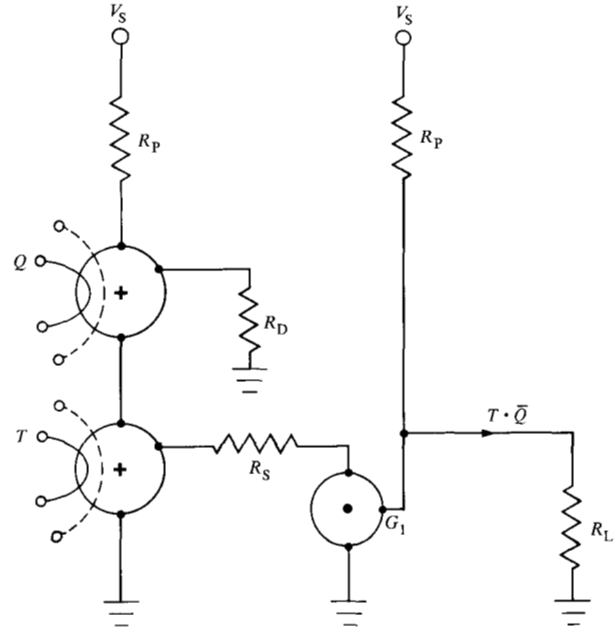

Figure 20 A CIL timed inverter circuit (V_S = 11.8 mV, R_P = 74.3 Ω, R_D = 16 Ω, R_S = 10 Ω, R_L = 12 Ω).

Timed inverter

The CIL circuits do not respond to the removal of control currents because they latch to the nonzero voltage state. This results in a logic inversion technique which is different from the conventional inverters. The timed inverter circuit shown in Fig. 20 utilizes a timing pulse, T, which is designed to become "1" only after the logic state of signal Q is determined. When T = "1," and if Q = "0," the output of the timed inverter circuit will be a "1"; whereas if Q = "1" the output will be a "0." The injection gate G_1 functions as a signal amplifier in this circuit. The nominal gate delay for the timed inverter is estimated to be 30 ps. It is possible to eliminate the need for inverters by iterative applications of D'Morgan's theorem until all the inversions apply only to the outputs of the latches where both true and complement signals are available.

Experimental delay measurements

The logic delays of the CIL circuits were experimentally measured on test chips using 2.5-μm nominal dimensions [2]. The chips were fabricated using the lead-alloy process described in this issue [15]. Because of processing variations the test samples differed from the nominal de-

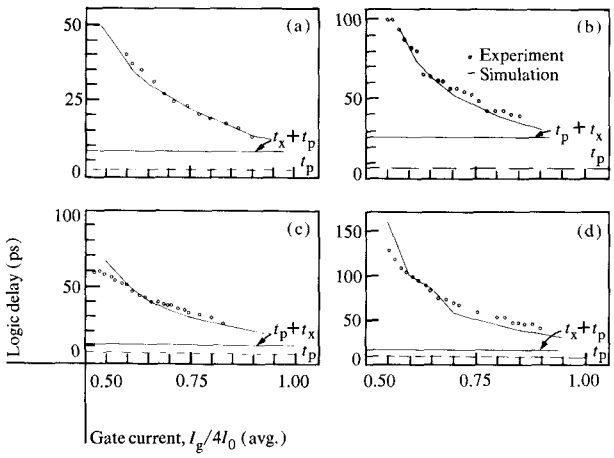

Figure 21 Comparison between the experimentally measured logic delay of CIL circuits and the delay estimates based on computer simulations as functions of the normalized gate current bias $I_g/I_m(0)$: (a) two-input OR ($\Delta I_0 = \pm 10\%$); (b) four-input OR ($\Delta I_0 = \pm 15\%$); (c) two-input AND ($\Delta I_0 = \pm 17\%$); and (d) four-input AND ($\Delta I_0 = \pm 10\%$).

Table 2 Comparison between the nominal design values and the experimentally obtained values of the logic design parameters.

Logic design variables	*Nominal design value*	*Test-chip value*
I_0 (μA)	50	65
Z_0 (Ω)	12	7.1
C_j (pf)	0.17	0.12
R_L (Ω)	12	13
L_m (pH)	10.8	9.8
L_x (pH)	52	46
$N_1 = I_{02}/I_{01}$*	3	3
$N_2 = I_{01}/I_{01}$**	5	7
V_m (mV)	27	27
V_g (mV)	3	3

*N_1 = ratio of the critical currents in the small injection gate.
**N_2 = ratio of the critical currents in the large injection gate.

Table 3 Experimentally measured logic delay of 2.5-μm CIL circuits.

Gate	*Fan-in*	*Fan-out*	*Fastest delay* $I_g(max)$	*Nominal delay* $I_g = 0.7\,I_m(0)$
2-OR	2	1	13	26
2-AND	4	1	26	32
4-OR	4	6	39	53
4-AND	8	2	42	63
Average	4.5	2.5	30	43.5

sign in several ways, as indicated in Table 2. The lower junction capacitance C_j, higher critical currents, and lower crossing inductance L_x helped to speed up the logic circuits. However, the overall effect of the variations in the processing parameter was to increase the logic delay over the nominal design because of lower line impedance Z_0 and lower mutual inductance L_m between the interferometer and the control lines. The delay measurements are compared with computer simulations in Fig. 21. The computer simulations were based on the test parameters listed in Table 2. The propagation delay, t_p, and the fan-out delay, $t_p + t_x$, are also indicated in Fig. 21.

The logic delay was measured across a chain of ten logic gates to permit the use of room-temperature high-speed sampling oscilloscopes. An example of the delay measurement for a chain of ten two-input OR gates is shown in Fig. 22. The photomicrograph of the delay test circuit is shown in Fig. 22(a). When input V_p = "0," the START signal travels through the chain of ten two-input OR gates before arriving at the output. When V_p = "1," the START signal is steered directly to the output, bypassing the ten two-input OR gates. Thus the time interval between the two output waveforms for V_p = "1" and V_p = "0" gives the total logic delay of the ten two-input OR gates. The example in Fig. 22(b) indicates an average logic delay of 13 ps/gate for the two-input OR gate. The fan-out in this example is one. This is the fastest measurement for the two-input OR gate obtained at the maximum gate current I_g(max) to which the delay chain could be biased without exceeding the threshold current $I_m(0)$. Due to the process variations, the critical currents of the ten logic gates in a chain were found to be distributed in a range I_0(avg) $\pm$ ΔI_0. The values of I_0(avg) and ΔI_0 were estimated from the composite threshold curve of the delay chain. The computer delay simulations were carried out for logic gates with critical current I_0(avg) and were compared with the average delay measured over ten gates. The highest gate current I_g(max) at which the delay chain could be operated was set equal to $4[I_0(\text{avg}) - \Delta I_0]$. The noise and the power supply disturbs were estimated to be small and hence were neglected in the computer simulations. The agreement between the measurements and the simulations shown in Fig. 21 is excellent, indicating the high accuracy of the models. The logic delay measurements are summarized in Table 3. The column "fastest delay" corresponds to the logic delay measured at the highest gate current I_g(max) to which the experimental delay chain could be biased. The column "nominal delay" corresponds to the logic delay measured at the nominal gate current level of 0.7 $I_m(0)$. With the aid of computer simulations the experimental logic delay for the nominal case $I_g = 0.7\,I_m(0)$ can be broken down into its basic components, as shown in Table 4. A comparison with Table 1 shows that the lower line impedance on the test chip resulted in an increase in the logic delay of 3.25 ps. The increase in the switching delay t_g of the test circuits is caused by the lower mutual inductance L_m. The

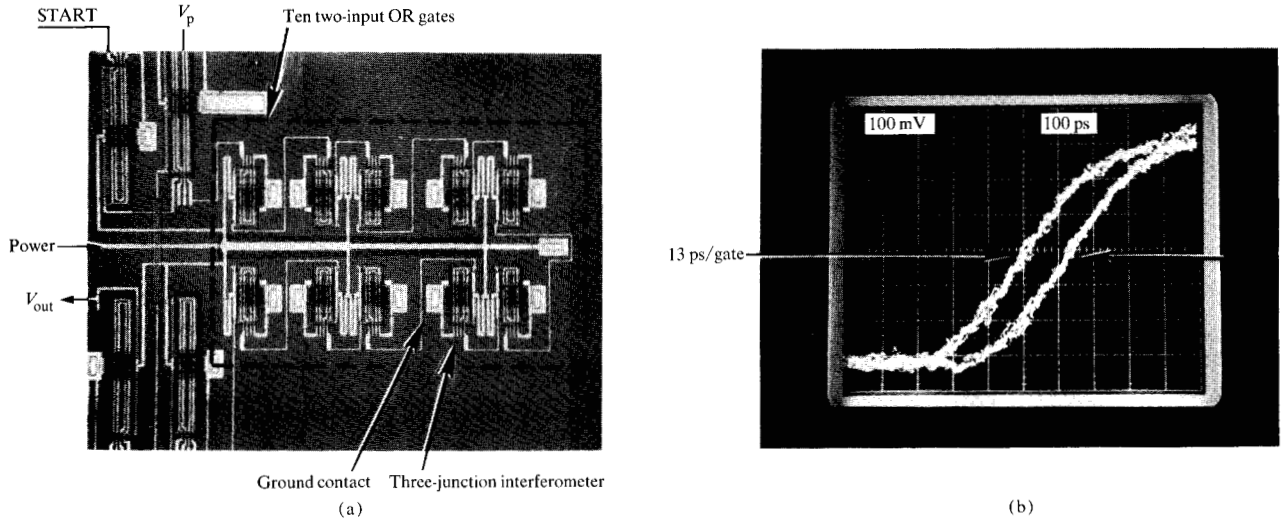

Figure 22 (a) Photomicrograph of a delay chain consisting of ten two-input OR gates. (b) Delay measurement of the same, indicating a logic delay of 13 ps/gate.

Table 4 Delay components and power dissipation of the experimental CIL test circuits for the nominal gate current $I_g = 0.7\ I_m(0)$.

Gate	*Total delay* t_D (ps)	*Turn-on & rise time* t_g (ps)	*Crossing delay* t_x (ps)	*Propagation delay* t_p (ps)	*Power dissipation* T_d (μW)
2-OR	26	17.1	6.5	2.4	1.9
2-AND	32	20	6.5	5.5	4.5
4-OR	53	27.1	19.5	6.4	4.3
4-AND	63	47.2	6.5	9.3	8.3
Mean	43.5	27.9	9.75	5.9	4.75

effect of the lower mutual inductance on t_g is more evident in the two- and four-input OR and the four-input AND gates, but less evident in the two-input AND gate which has higher gain. The two-input AND gate is in fact faster than the nominal design because of the lower junction capacitance C_j on the test chips.

Summary

Josephson Current Injection Logic (CIL) is based on two types of superconducting circuits. The first circuit is a magnetically controlled three-junction interferometer which provides isolation and the two-input OR function. The second circuit is a directly coupled injection gate which provides gain and the two-input AND function. The designs of the three-junction interferometers and the injection gates were described and optimized with respect to their gain, operating margins, and process tolerances.

The CIL circuits consist of two- and four-input OR and AND gates and a timed inverter circuit. The AND gates have a two-input OR gate at each input. Thus the four-input AND gate, for example, has a total fan-in of eight. The two-input AND gate also performs the EXCLUSIVE-OR function. The CIL circuits are latching, requiring an ac power supply. All the logic circuits have serial fan-out capability. In addition, the four-input OR and AND gates have two parallel output lines.

The nominal logic delay averaged over the four logic circuits is estimated at about 36 ps/gate for a fan-out of three. The corresponding power dissipation is 3.4 μW and the power-delay product is 175×10^{-18} joules. The two factors which affect the logic delay most strongly are the junction capacitance and the margins on the critical current, $\Delta I_m(0)$, which controls how high a gate current can be used to bias the three-junction interferometers.

The CIL delay estimates have been verified experimentally. The experimentally measured logic delay averaged over the four logic gates is 30 ps/gate at the maximum

gate current and 43.5 ps/gate at the nominal gate current. The difference between the measured and the projected logic delay is attributed to variations in the processing parameters from the nominal design. The experiments are in excellent agreement with computer simulations once the device models are modified to match the process parameters obtained on the test chip.

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